# EE/CprE 4910 – sdmay25-26
# Week 7 Report
# 10/24/2024 - 10/31/2024

Cost-Effective and Easily Configurable High Voltage Motor Controllers for Automotive Use
PRISUM Solar Car Club, Jonah Frosch
Nathan Neihart, Cheng Huang

## Summary

We've started to test some of our software and our hardware is starting to see simulations. After meeting with our advisors, it became very clear that we needed to get way more organized to handle things. This is organizing our timeline, our resources, and our goals in order to have something structured to present at the end of the semester. Going forward, we will work with that in mind.

## Accomplishments

- Tested dev board software on Mitsuba motor – Bryce, Gavin
    - Fixed project bugs
    - Test on smaller motor which faulted for under volt
- Fixed spare Mitsuba motor
- Ordered spare HALL sensor board as a backup for the Mitsuba motor
- Testing gate drivers with transistors in LTspice (see **Figure 1**)
    - Identified the transistor for our rev 1 design, the IRFP4668
    - Identified gate driver for rev 1 design, the IR2132S

## Pending Issues

Due to time restrictions, we need to pin down exactly what we plan to have completed at the end of the semester and for the panel presentation. Our biggest concern with this is hardware lead times of custom Printed Circuit Boards from Detroit.

## Individual Contributions

| Member | Contributions | Week Hours | Cumulative Hours |
|---|---|---|---|
| Gavin Patel | Generated new motor params, skeleton code | 7 | 33 |
| Bryce Rega | Tested example, wrote some skeleton code | 7 | 37 |
| Marek Jablonski | Created simulation setup and specified rev 1 gate driver | 8 | 37 |
| Jonah Frosch | Built dev board test rig and fixed HAL sensor | 7 | 36.1 |
| Long Yu | Ordered hall sensor, fixed and tested the issue | 6 | 34 |

## Upcoming Week

- Reverse engineer PWM functions by header file and plan code for MVP
- Skeleton general application functions for MVP
- Finish headers for low-level firmware (supports multiple chips with copies of files)
- Design first fully featured custom board
    - First Schematic and board layout
    - May have significant issues but should be functional
- Put together current Project Summary for advisor presentation
- Develop the next sections of the Design Document

## Advisor Meeting Summary

- Overall criticism about our progress so far, need to hurry our simulation and design up
- We need to worry about voltage spiking due to inductive effects
- Neihart: We need to schedule more meetings so they can properly address us. Meet weekly with proper updates, making it clear what we have accomplished and goals for the upcoming week. Meet this time Wednesday every week, and make slides for them so we have properly assessed. Need to start thinking about what we are going to present. Screenshots of results, block diagram/schematic, screenshots of oscilloscope. Specifications that we want to meet, along with overview of individual components. Along with the expected deliverables, and plan.
- Block diagram, Specific deliverables, update of hardware architecture for next week. Software doesn't care about specific code, wants to see more higher-level architecture or actual results. Block diagram here as well.
- Neihart wants plots with axis labeled, is fine with output from block diagrams.
    - Likes having a list of milestone projects for the next few weeks and how we plan to accomplish those
- Cheng wants to see specifications and applications to see how we got those. Wants to see bigger picture of our project.
- Overall wants to see target for the next few weeks. Wants a solid idea of what we are going to attempt to accomplish by the end of the semester.

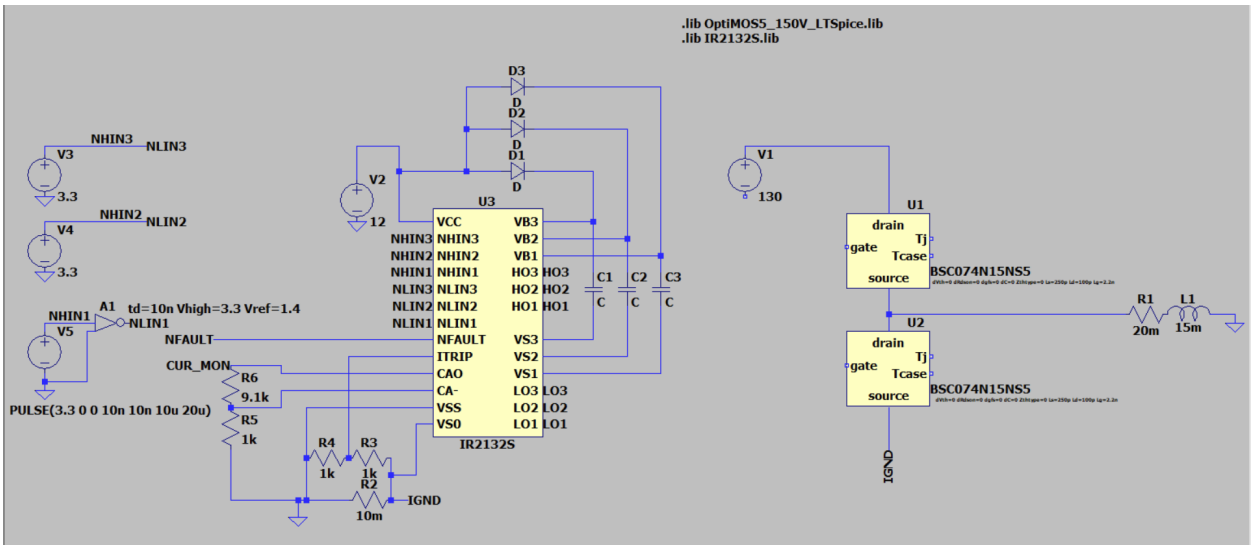


*Figure 1. A simulation schematic setup for testing gate drivers.*